

**WHAT IS CLAIMED IS:**

1           1.       A delta-sigma modulation system comprising:  
2           an M-order filter to process input data, wherein M is greater than or equal to 3;  
3           an N-order filter that is stable during overload conditions; and  
4           a quantizer system coupled to the M-order and N-order filters to receive input  
5           data from the M-order and N-order filters, provide quantized feedback  
6           data,  $q_M$ , to the M-order filter, provide quantized feedback data,  $q_N$ , to  
7           the N-order filter, and provide two state quantization output data  $q$ ,  
8           wherein  $q = q_M + q_N$ .

1           2.       The delta-sigma modulation system of claim 1 wherein a maximum  
2           value of feedback data  $q_M$  is greater than a maximum value of output data  $q$ , and a  
3           minimum value of feedback data  $q_M$  is less than a minimum value of output data  $q$ .

1           3.       The delta-sigma modulation system of claim 1 wherein  $q$  is an element  
2           of the logical value set  $[+1, -1]$ , a maximum value of feedback data  $q_M$  is greater than  
3            $+1$ , and a minimum value of feedback data  $q_M$  is less than  $-1$ .

1           4.       The delta-sigma modulation system of claim 3 wherein feedback data  
2            $q_M$  and  $q_N$  are integers.

1           5.       The delta-sigma modulation system of claim 3 wherein feedback data  
2            $q_M$  and  $q_N$  are real numbers including non-integers.

1           6.       The delta-sigma modulation system of claim 1 wherein N equals 2.

1           7.       The delta-sigma modulation system of claim 1 further wherein the  
2           input signal is a decimated version of a digital audio signal.

1           8.       The delta-sigma modulation system of claim 1 wherein the input signal  
2           is a digital input signal.

1           9.     A digital signal processing system having a delta-sigma modulator  
 2 with stability protection during quantizer overload conditions, the system comprising:  
 3           an M-order loop filter to process a sum of input data and feedback data,  $q_M$ ,  
 4           wherein M is more than two;  
 5           an N-order loop filter to process feedback data,  $q_N$ , wherein N is selected from  
 6           the group consisting of one and two;  
 7           a rules based 1-bit quantizer to process output data from the N-order loop filter  
 8           and M-order filter and to provide  $q_M$ ,  $q_N$ , and 1-bit quantized output  
 9           data,  $q$ , wherein  $q = q_M + q_N$ , and  $q_{Mmax}$  is greater than the maximum  
 10           value of  $q$  and  $q_{Mmin}$  is less than the minimum value of  $q$  to maintain  
 11           stability of the M-order loop filter during overload conditions.

1           10.    The digital signal processing system of claim 9 wherein overload  
 2 conditions include conditions wherein a significant probability exists that input data to  
 3 the quantizer will cause the M-order filter to become unstable if  $q_M$  does not exceed  
 4 the maximum range of  $q$ .

1           11.    A digital signal processing system comprising:  
 2           an M-order filter to process input data, wherein M is greater than 2;  
 3           an N-order filter that is stable during overload conditions; and  
 4           a quantizer system coupled to the M-order and N-order filters to receive input  
 5           data from the M-order and N-order filters, provide quantized feedback  
 6           data to the M-order filter, provide quantized feedback data to the N-  
 7           order filter, and provide two state quantization output data, wherein the  
 8           quantization output data approximately equals the feedback data to the  
 9           M-order filter plus the feedback data to the N-order filter.

1           12.    The digital signal processing system of claim 11 wherein a maximum  
 2 value of feedback data is greater than a maximum value of output data, and a  
 3 minimum value of feedback data is less than a minimum value of output data.

1           13.     A method of maintaining stability of a 1-bit delta-sigma modulation  
2 system under overload conditions, the method comprising:  
3           providing quantized output data using output data of an M-order filter and  
4           output data of an N-order filter, wherein M is greater than or equal to 3  
5           and the N-order filter is stable under overload conditions;  
6           providing feedback data,  $q_M$ , to the N-order filter;  
7           providing feedback data  $q_N$  to the N-order filter; and  
8           providing 1-bit quantization output data,  $q$ , wherein  $q$  equals  $q_N + q_M$ .

1           14.     The method of claim 13 wherein a maximum value of feedback data  
2  $q_M$  is greater than a maximum value of output data  $q$ , and a minimum value of  
3 feedback data  $q_M$  is less than a minimum value of output data  $q$ .

1           15.     The method of claim 14 wherein feedback data  $q_M$  and  $q_N$  are integers.

1           16.     The method of claim 14 wherein feedback data  $q_M$  and  $q_N$  are real  
2 numbers including non-integers.

1           17.     The method of claim 13 wherein  $q$  is an element of the logical value  
2 set  $[+1, -1]$ , a maximum value of feedback data  $q_M$  is greater than  $+1$ , and a minimum  
3 value of feedback data  $q_M$  is less than  $-1$ .

1           18.     The method of claim 13 wherein  $N$  equals 2.

1           19.     The method of claim 13 further wherein the input signal is an  
2 oversampled version of a digital audio signal.

1           20.     The method of claim 13 further comprising:  
2 receiving a digital input signal;  
3 providing the digital input signal to the N-order filter; and  
4 converting the 1-bit quantization output data into encoded audio data.

1           21.     A method of maintaining stability of a 1-bit delta-sigma modulator  
 2 during overload conditions, wherein the 1-bit delta-sigma modulator comprises a  
 3 quantizer, an M-order loop filter, and an N-order loop filter, the method comprising:  
 4           providing 1-bit output data,  $q$ , based on input data from an M-order loop filter  
 5                     and an N-order loop filter, wherein  $M$  is greater than or equal to three  
 6                     and  $N$  is selected to provide stability to the delta-sigma modulator  
 7                     during overload conditions;  
 8           detecting an overload condition of a quantizer;  
 9           providing appropriate feedback data,  $q_M$ , for the M-order loop filter to enable  
 10                     the M-order loop filter to remain stable during the overload conditions,  
 11                     wherein a maximum value of feedback data  $q_M$  is greater than the  
 12                     maximum value of output data  $q$ ; and  
 13           providing compensating feedback data,  $q_N$ , for the N-order loop filter to  
 14                     maintain an acceptable gain level of the quantizer.

1           22.     The method of claim 21 further comprising:  
 2                     determining  $q_M$  and  $q_N$  using a predetermined set of rules.

1           23.     The method of claim 21 wherein  $q = q_M + q_N$ .